

**ABSTRACT**

To prevent a timing shift of a clock and data supplied to a driver IC.

A driver 1011 includes a phase adjustment circuit 201 for  
5 receiving via input terminals a clock and data outputted from  
a controller 103, latching received data with the clock adjusted  
to a 50-percent duty ratio, and outputting as phase-adjusted  
signals the data having the latched data further latched by  
synchronizing it with a delay clock having the  
10 duty-ratio-adjusted clock delayed by  $(\pi/2)$  and the clock of the  
50-percent duty ratio.